SERVICE MANUAL

1571 DISK DRIVE

Preliminary

OCTOBER 1986 **PN-314002-04**

commodore COMPUTERS

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Commodore Business Machines, Inc.
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SPECIFICATIONS

COMMODORE 1571 DISK DRIVE

GENERAL FEATURES

- 5¼'' Floppy Disk Drive
- Supports Fast Data Transfer Rates
- Two Serial Ports for Adding Peripherals
- Software Disk Format Selectable
- Comes with Serial and Power Cables
- Compatible with Commodore 128, Commodore 64, and Plus/4 Computers

SYSTEM FEATURES

- Built-in 6502 Microprocessor
- 2K RAM
- 32K ROM
- Built in DOS
- Program Load Transfer Rates
  - 300 cps under C64 Control
  - 5200 cps Max under C128 Control (Burst Rate)
  - 5200 cps Max under CP/M® Control (Burst Rate)

MEDIA CHARACTERISTICS

- Commodore Standard (GCR)
- Double Sided/Single Density
- 350K Storage Capacity (Formatted)
- Compatible with 1541 Disk Drive
- Supports Program, Sequential, Relative and User Files

- CP/M® Compatible (MFM)
- Single or Double Sided/Double Density Formats
- Up to 410K Storage Capacity (Formatted)
- Read/Write Compatible with Kaypro,® Osborne,® IBM,® CP/M 86, Epson® QX-10 and Numerous Other Formats
- Supports Most CP/M® Files

INPUTS/OUTPUTS

- Two Serial Ports
- Power Connector

POWER REQUIREMENTS

- 117 Volts Ac, 60 Hz, Less than 25 Watts

Specifications subject to change without notice.
CP/M is a registered trademark of Digital Research, Inc.
KayPro is a registered trademark of Kaypro, Inc.
Osborne is a registered trademark of Osborne Computer Corporation.
IBM is a registered trademark of International Business Machines Corp.
Epson is a registered trademark of Epson Corporation.

PARTS LIST
1571

PLEASE NOTE: Commodore part numbers are provided for reference only and do not indicate the availability of parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Approved cross-references for TTL chips, Transistors, etc. are available in manual form through the Service Department. Unique or non-standard parts will be stocked by Commodore and are indicated on the parts list by a "C".

TOP CASE ASSY

Top Case	C 310508-01

BOTTOM CASE ASSY

Bottom Case	C 310509-01
PCB Assembly	C 310420-01
Power Supply Assembly	C 250772-01
Drive Assembly — Newtronics	C 252083-01
Drive Assembly — Alps	C 252092-01
PCB Shield	C 252069-01
PCB Insulation Sheet	C 252070-01

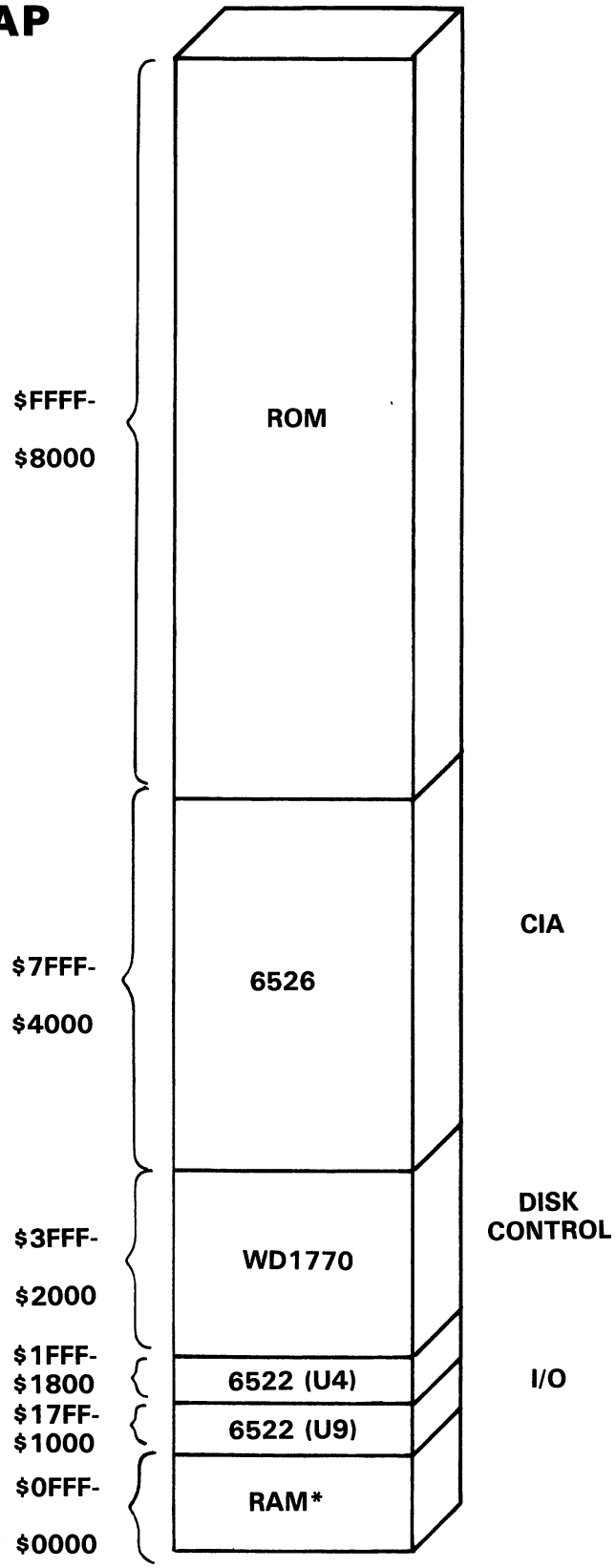
FRONT CASE ASSEMBLY

Front Bezel — Alps	C 252086-01
Front Bezel — Newtronics	C 310507-01
Disk Eject Lever	C 252050-01
LED Assembly	C 250754-04
LED Clip	C 252013-01
Nameplate	C 310411-01

ACCESSORIES

Users Manual	C 252095-01
Demo Disk	C 252093-01
Power Cord	C 252164-01 sub: C 903508-04
6-Pin Din Cable	C 252159-01 sub: C 1540027-01

MEMORY MAP



*ONLY 2K OF RAM SPACE AVAILABLE IN THE 1571

ADDRESS DECODING IS ACCOMPLISHED BY THE 64H157 GATE ARRAY.

20 PIN GATE ARRAY 1541B AND 1571

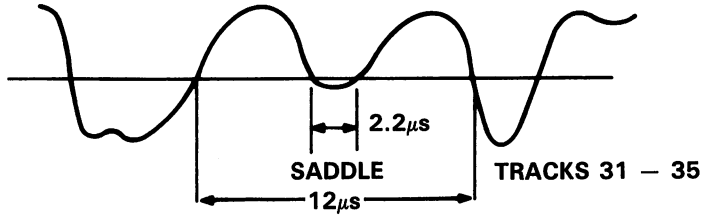
The 20 pin gate array used in the 1541B and 1571 disk drives is designed to work in conjunction with the 40/42 pin gate array also used in these drives. As illustrated in the block diagram, this I.C. controls 3 operations:

Address Selector The function of the address selector is to produce ROM, RAM and I/O chip select signals by decoding the addresses A10, A12, A13, A14 and A15. The system clocks are not gated with the address lines in this I.C. All chip select outputs are ACTIVE LOW.

Address decode Map:

RAME	0000 — 0FFF
I02	1000 — 1FFF
CS1	2000 — 3FFF
I01	1800 — 1BFF
CS2	4000 — 7FFF
ROME	C000 — FFFF

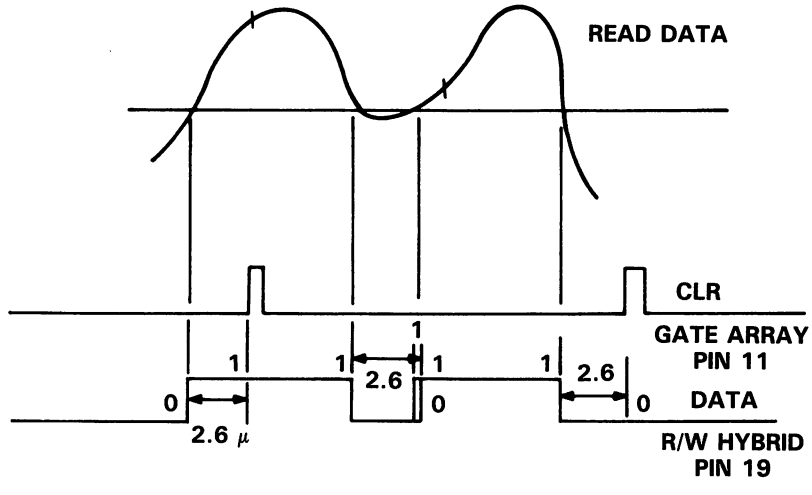
Saddle Canceler This correction signal is generated during the period that the data pattern is two consecutive zeros. With the Commodore GCR type recording format, a problem occurs in the waveform of the read signal. In the worst case pattern of 1001, a saddle condition will occur as illustrated below.



The worst case saddle will occur in tracks 31 to 35 and if not compensated for, will result in a read error. In the original 1541 drives, a one-shot was used to correct the condition; however, in this gate array it is corrected digitally.

The data output line, pin 19, of the R/W Hybrid's data comparitor is fed to the data input line, pin 3, of this gate array.

The data is then compared with the last data value which has been latched by the gate array, 2.6μS after the rising or falling edge of the data line. If the current data value differs from the previous data value, the clear line is set to a high level for a duration of 63nS. If the values are the same, the clear line is not set.

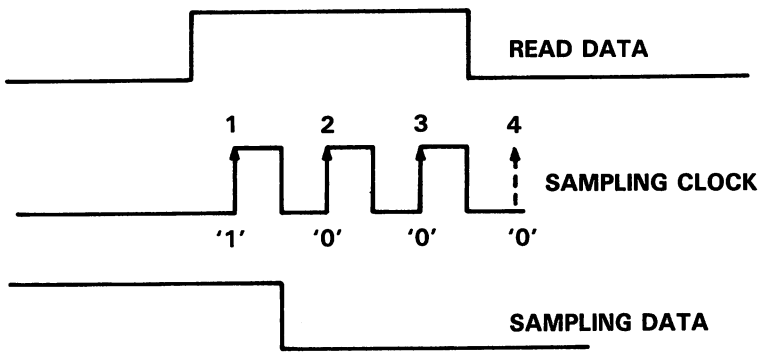


It takes 2.56 to 2.62μS to cancel the saddle. If the saddle should be longer than this length of time, the saddle can not be corrected and will result in a read error. Also, if the time for correcting the saddle is set for a longer time interval, the clear signal will not be set when the data is equal to 11. Therefore, approximately 2.6μS the most suitable time setting for saddle correction.

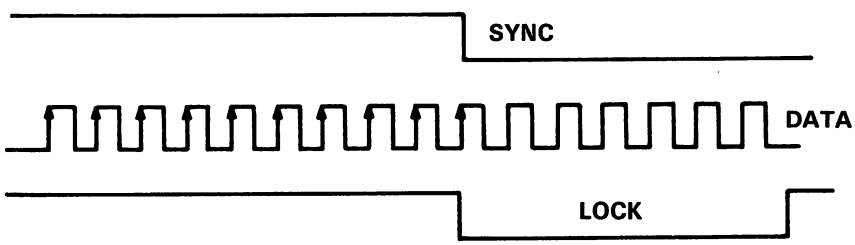
Note: The minimum bit rate for tracks 1 — 17 is equal to 2.6 μsec. If this time should become less due to motor speed, the SYNC signal cannot be recognized on the outer tracks resulting in error.

Motor Speed Compensator (PLL)

This gate array detects the motor speed and generates an internal data sampling clock signal that matches with the motor speed. (See below)

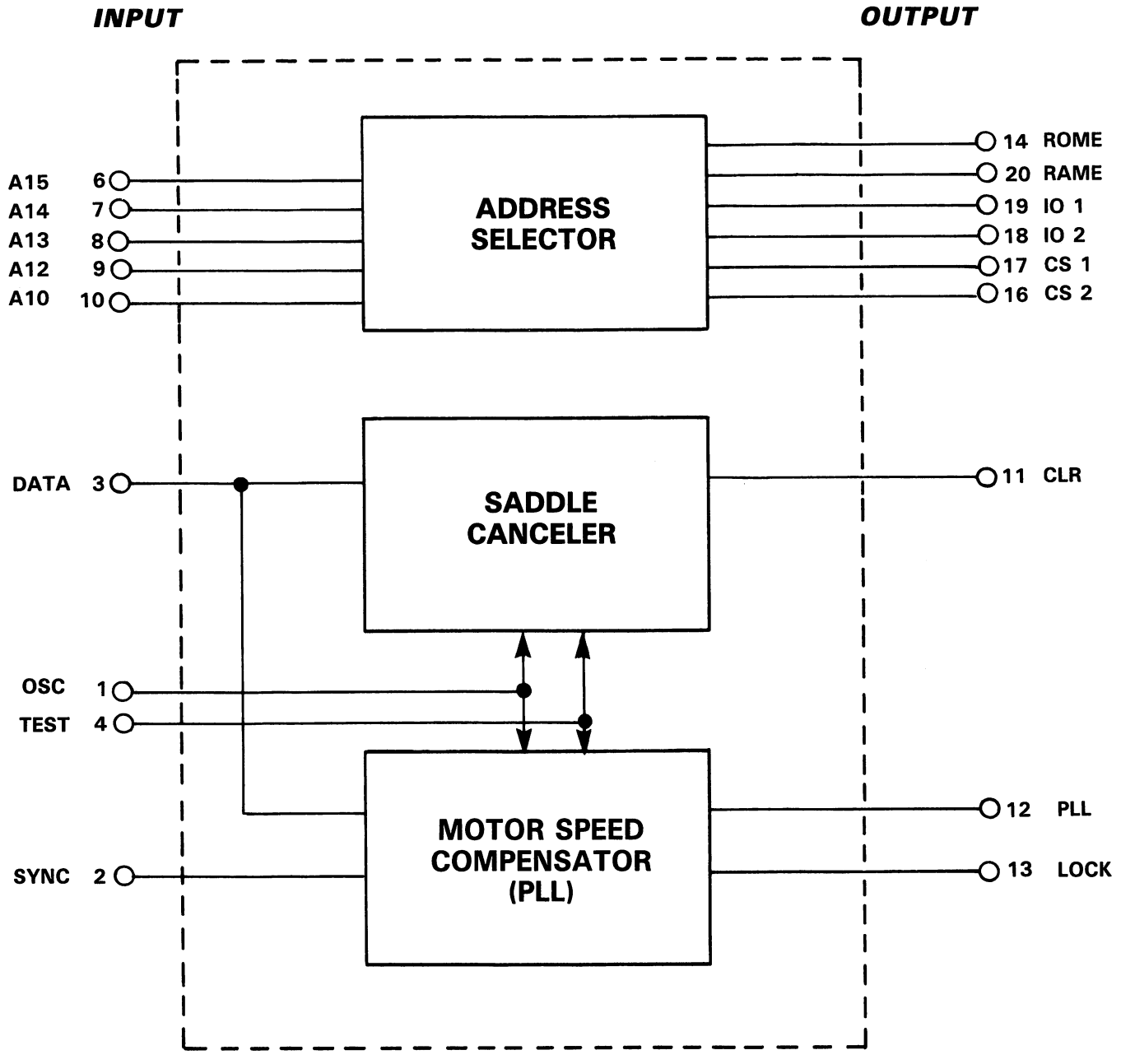


When the SYNC signal goes to the low level, the LOCK signal goes false and the sampling clock is switched to the internal clock signal of the gate array. Once the PLL has sampled the data one's, the LOCK signal will go high to indicate that the output of the PLL is valid. If the PLL cannot lock on, the internal clock signal will be used and the LOCK signal will remain at the low level. This can occur when the stepper is still moving or the spindle motor is not up to speed yet. In short, this allows the reading of data independent of motor speed within the lock on limits of the PLL.

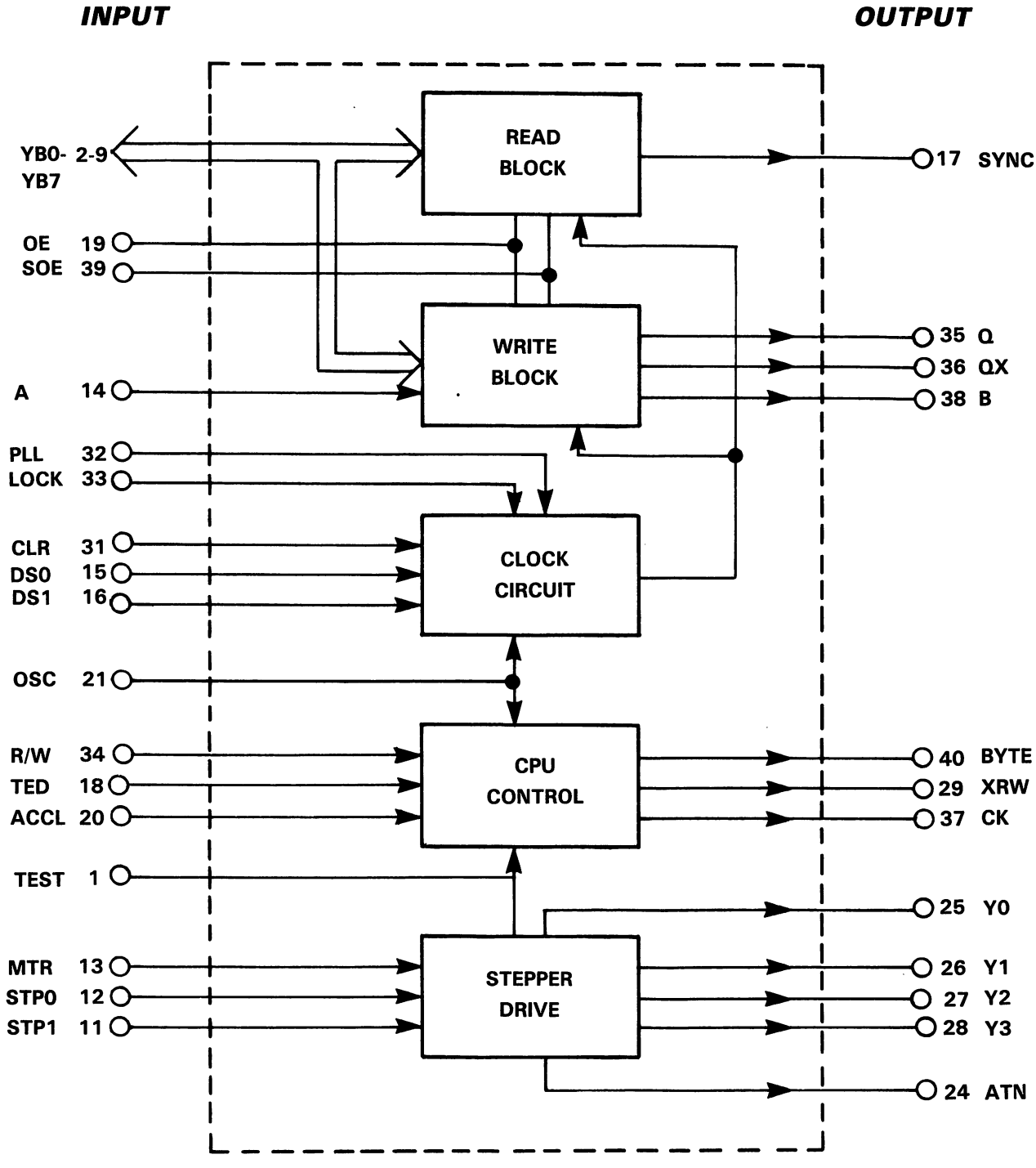


The 1571 runs on the SYSTEM CLOCK and does not implement the LOCK signal.

251829
BLOCK DIAGRAM
20 PIN GATE ARRAY FOR 1541B/1571

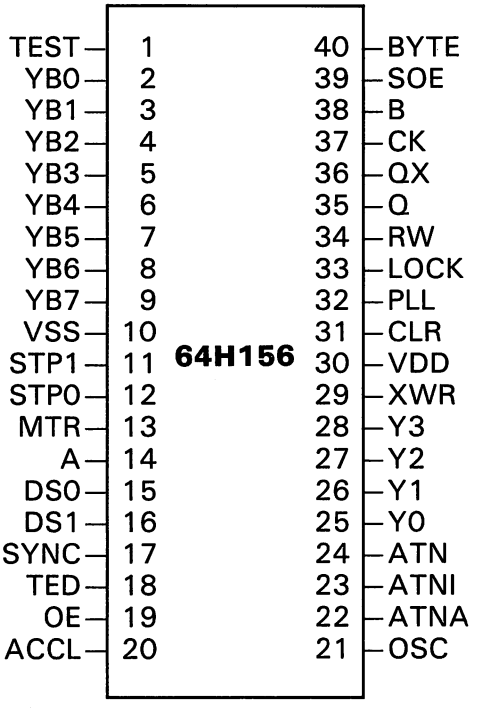


251828
BLOCK DIAGRAM
40/42 PIN GATE ARRAY FOR 1541B/1571



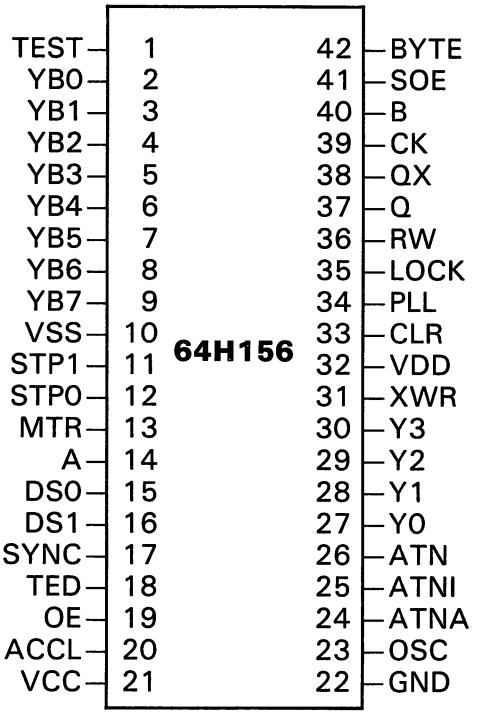
40/42 PIN GATE ARRAY

PIN ASSIGNMENT



—01 SHOWN

PIN ASSIGNMENT

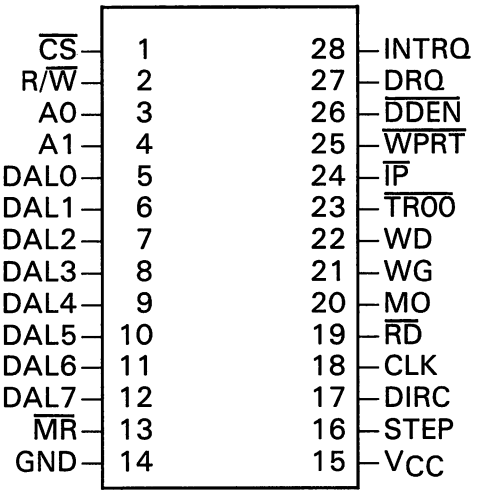


—02 SHOWN

40 PIN	42 PIN	DESC	FUNCTION
1	1	TEST	Input used in design verification.
2-9	2-9	YB0-YB7	Data input/output lines for read/write operation.
10	10	Vss	Ground.
11,12	11,12	STP0,STP1	Input to stepper driver.
13	13	MTR	Control line used to activate the stepper motor.
14	14	A	Write protect input. Indicates disk is write protected.
15,16	15,16	DS0,DS1	Inputs used to produce the binary count for the frequency divide ratio.
17	17	SYNC	Sync output.
18	18	TED	A low input clears the BYTE line in 2 MHz mode. A high sets 1541 mode.
19	19	OE	Input to read/write block to set mode. 0 for Write, 1 for Read.
20	20	ACCL	Input select line for the CPU clock. 0 for 1541 - 1 MHz, 1 for 1571 - 2 MHz.
XX	21,22		N/C
21	23	OSC	16 MHz clock input.
22	24	ATNA	Attention acknowledge input.
23	25	ATNI	Attention line input from serial bus.
24	26	ATN	Attention data input from serial bus.
25-28	27-30	Y0-Y3	Control output lines for the 4 phases of the stepper motor.
29	31	XRW	RAM write enable output.
30	32	Vcc	+5VDC.
31	33	CLR	High input when the read data is logical 1.
32	34	P11	Input from the 20 pin gate array. Clock compensation.
33	35	LOCK	Indicates the PLL LOCK status. When logical 1, PLL is locked. When 0, the internal clock is used for sampling data.
34	36	R/W	R/W select input.
35,36	37,38	Q,Qx	Write pulse outputs.
37	39	CK	Clock select output — 1 or 2 MHz.
38	40	B	Write enable output.
39	41	SOE	Enable byte input.
40	42	BYTE	Data latched output.

WD1770/1772
5-1/4"FLOPPY DISK CONTROLLER/FORMATTER

PIN ASSIGNMENT

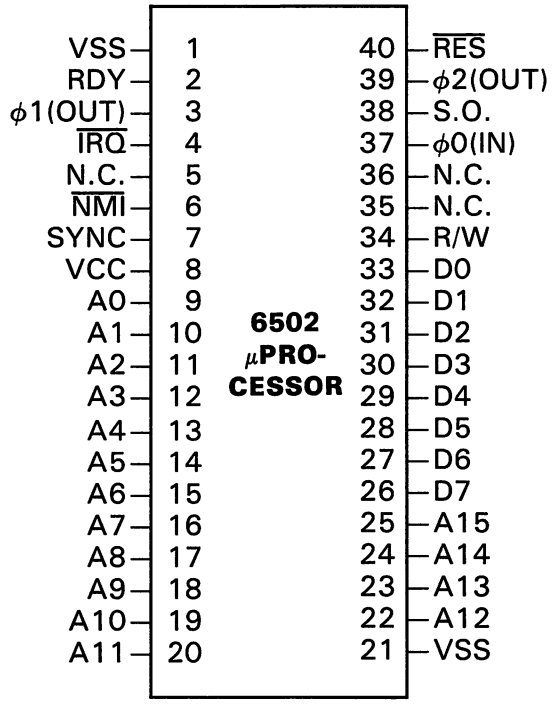


1	CS	CHIP SELECT	A logic low on this input selects the chip and enable Host communication with the device.
2	R/W	READ/WRITE	A logic high on this input controls the placement of data on the D0-D7 lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	A0,A1	ADDRESS 0,1	These two inputs select a register to Read/Write data:
5-12	DAL0-DAL7	DATA ACCESS LINES 0 THRU 7	Eight bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by CS and R/W. Each line will drive one TTL load.
13	MR	MASTER RESET	A logic low pulse on this line resets the device and initializes the status register (internal pull-up).
14	GND	GROUND	Ground.
15	V_{CC}	POWER SUPPLY	+5V ±5% power supply input.
16	STEP	STEP	The Step output contains a pulse for each step of the drive's RW head. The WD1770 and WD1772 offer different step rates.
17	DIRC	DIRECTION	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLK	CLOCK	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHZ ±1%.
19	RD	READ DATA	This active low input is the raw data line containing both clock and data pulses from the drive.
20	MO	MOTOR ON	Active high output used to enable the spindle motor prior to read, write or stepping operations.
21	WG	WRITE GATE	This output is made valid prior to writing on the diskette.
22	WD	WRITE DATA	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	TR00	TRACK00	This active low input informs the WD1770 that the drive's R/W heads are positioned over Track zero (internal pull-up).
24	IP	INDEX PULSE	This active low input informs the WD1770 when the physical index hole has been encountered on the diskette (internal pull-up).
25	WPRT	WRITE PROTECT	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up).
26	DDEN	DOUBLE DENSITY ENABLE	This input pin selects either single (FM) or double (MFM) density. When DDEN = 0, double density is selected (internal pull-up).
27	DRQ	DATA REQUEST	This Active high output indicates that the data register is full (on a READ) or empty (on a Write operation).
28	INTRQ	INTERRUPT REQUEST	This Active high output is set at the completion of any command or reset or read of the status register.

CS	A1	A0	R/W = 1	R/W = 0
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg

6502 MICROPROCESSOR

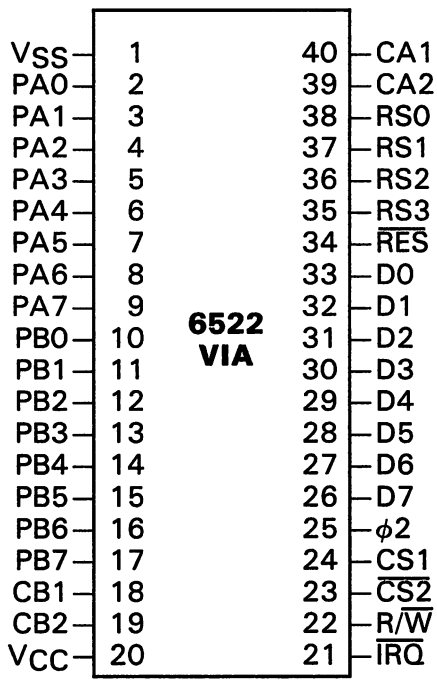
PIN ASSIGNMENT



1,21	VSS	DC ground.
2	RDY	Ready. TTL level input, used to DMA the 6502. The processor operates normally while RDY is high. When RDY makes a transition to the low state, the processor will finish the operation it is on, and any subsequent operation if it is a write cycle. On the next occurrence of read cycle the processor will halt, making it possible to tri-state the processor to gain complete access to the system bus.
3	φ1 OUT	Phase 1 clock output.
4	IRQ	The Interrupt Request input is a request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request. At that time, the interrupt mask in the Status Code Register will be examined. If the interrupt mask is not set, the processor will begin an interrupt sequence. The Program Counter and the Processor status register will be stored on the stack and the interrupt disable flag is set so that no other interrupts can occur. The processor will then load the program counter from the memory location $FFFE and $FFFF.
6	NMI	The Non-Maskable Interrupt Request is a negative-edge sensitive request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request.
7	SYNC	The SYNC output is used in conjunction with RDY to allow single instruction execution.
8	VDD	5VDC input.
9-20	A0-A15	Address bus outputs. Unidirectional bus
22,25		used to address memory and I/O devices.
26,33	D0-D7	Bi-directional bus for transferring data to and from the device and the peripherals.
34	R/W	The read/write line is a TTL level output from the processor to control the direction of data transfer between the processor and memory, peripherals, etc. This line is high for reading memory and low for writing.
37	φ0	Phase 0 clock input.
38	S.O.	Set Overflow flag. A negative going edge sets the overflow bit in the status code register.
39	φ2	Phase 2 clock output.
40	RES	The Reset input is used to reset or start the μprocessor from a power down condition. During the time that this line is held low, writing to or from the μprocessor is inhibited. When a positive edge is detected on the input, the μprocessor will immediately begin the reset sequence. After a system initialization time of 6 cycles, the mask interrupt flag will be set and the processor will load the program counter from the contents of the memory locations $FFFC and $FFFD. This is the start location for program control. After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least 2 cycles. At this time the R/W line will become valid.

6522
VERSATILE INTERFACE ADAPTOR (VIA)

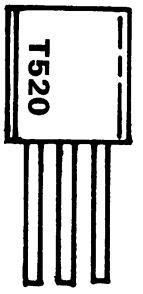
PIN ASSIGNMENT

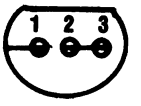


1	VSS	Ground.
2-9	PA0-PA7	Peripheral I/O Port A.
10-17	PB0-PB7	Peripheral I/O Port B.
18,19	CB1, CB2	Peripheral B Control Lines.
20	VCC	+5VDC.
21	IRQ	Interrupt Request.
22	R/W	Read/Write.
23,24	CS1, CS2	Chip Select.
25	φ2	Phase 2 Internal Clock.
26-33	D0-D7	Data Bus
34	RES	Reset Input, Low Active.
35-38	RS0-RS3	Register Select Inputs.
39,40	CA1, CA2	Peripheral A Control Lines.

T520
VOLTAGE DETECTOR I.C.

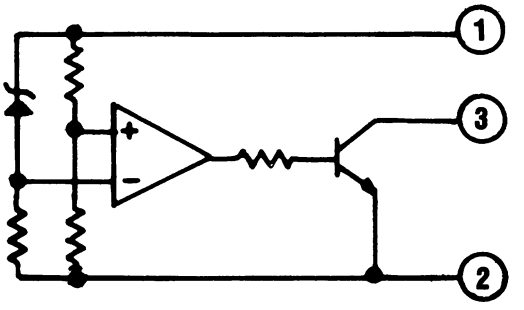
PIN CONFIGURATION





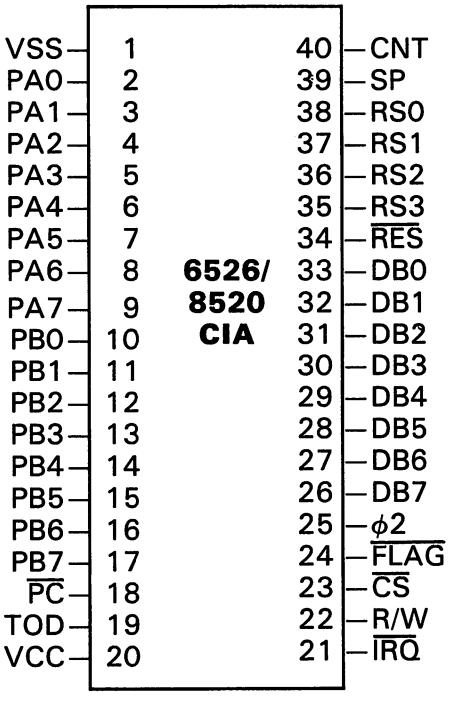
BOTTOM VIEW

EQUIVALENT CIRCUIT



6526/8520
COMPLEX INTERFACE ADAPTOR

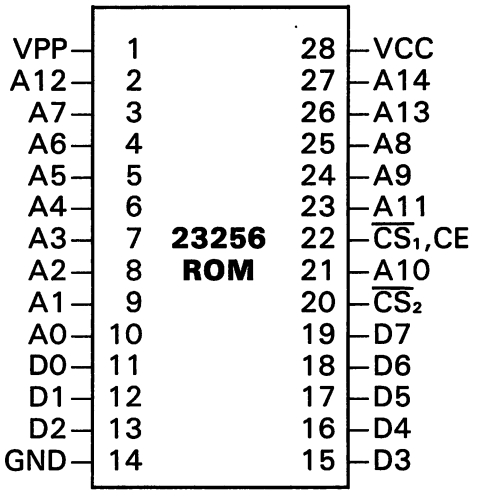
PIN ASSIGNMENT



1	VSS	Ground Connection.
2-9	PA0-PA7	Parallel port A signals. Bidirectional parallel port.
10-17	PB0-PB7	Parallel port B signals. Bidirectional parallel port.
18	PC	Handshake output. A low pulse is generated after a read or write on port B.
19	TOD	Time of day clock input. Programmable 50hz or 60hz input.
20	VCC	5VDC input.
21	IRQ	Interrupt output to microprocessor.
22	R/W	READ/WRITE input from microprocessor's R/W output.
23	CS	Chip select input. A low pulse will activate CIA.
24	FLAG	Negative-edge sensitive interrupt input. Can be used as a handshake line for either parallel port.
25	φ2	φ2 clock input.
26-33	DB0-DB7	Bidirectional data bus.
34	RES	Low active reset input. Initializes CIA.
35-38	RS0-RS3	Register select inputs. Used to select all internal registers for communications with the parallel ports, time of day clock, and serial port (SP).
39	SP	Serial Port bidirectional connection. An internal shift register converts microprocessor parallel data into serial data, and visa-versa.
40	CNT	Count input. Internal timers can count pulses applied to this input. It is used for frequency dependent operations.

23256
32K X 8 ROM

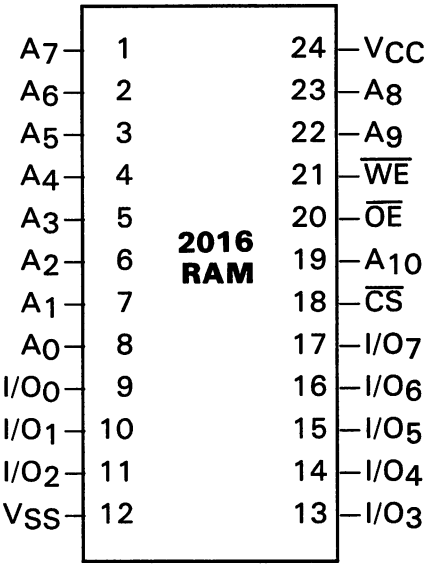
PIN ASSIGNMENT



1	VPP	5VDC.
2-10, 21, 23-27	A0-A14	Address Bus Inputs.
11-13, 15-19	D0-D7	Data Outputs.
14	GND	Ground.
20	CS_2	Chip Select.
22	CS_1, CE	Output Enable.
28	VCC	5VDC Input.

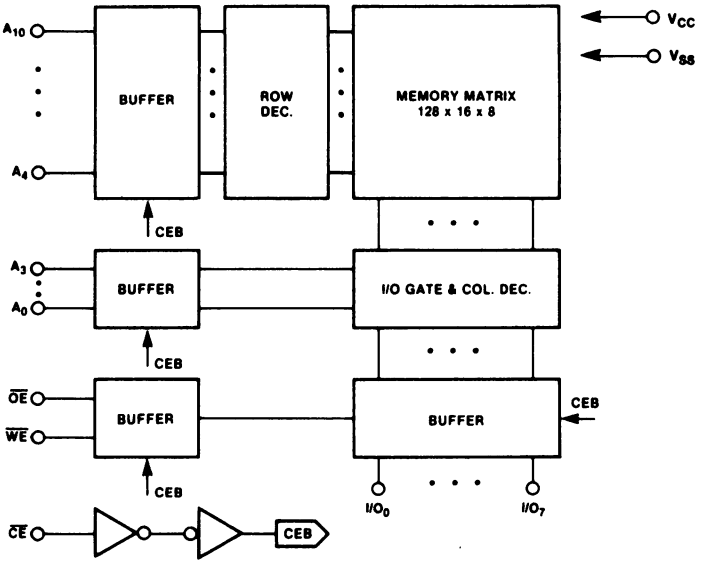
2016
2K X 8 STATIC RAM

PIN ASSIGNMENT



1-8, 19, 22 23	A_0-A_{10}	Address Bus Inputs.
9-11, 13-17	I/O_0-I/O_7	Common Data Input/Output Lines.
12	V_{SS}	Ground.
18	CS	Chip Select Enable, Low Active.
20	OE	Output Enable, Low Active.
21	WE	Write (Input) Enable, Low Active.
24	V_{CC}	5VDC Input.

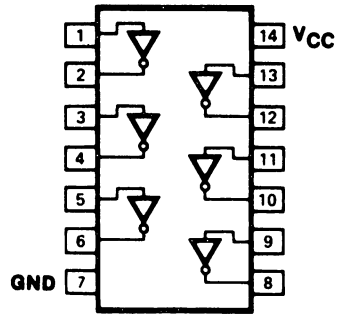
Functional Diagram



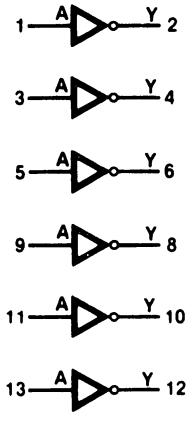
COMMON I.C.'S
PIN ASSIGNMENTS AND LOGIC

7406
HEX INVERTER BUFFER/DRIVER (OPEN COLLECTOR)

PIN ASSIGNMENT



LOGIC DIAGRAM



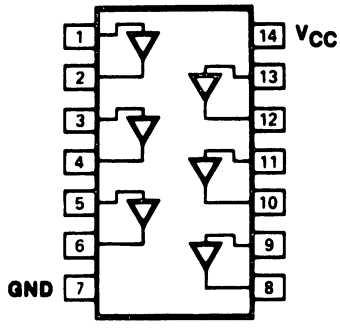
TRUTH TABLE

INPUT	OUTPUT
A	Y
H L	L H

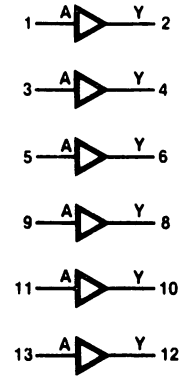
H = HIGH voltage level
L = LOW voltage level

7407
HEX BUFFER/DRIVER (OPEN COLLECTOR)

PIN ASSIGNMENT



LOGIC DIAGRAM



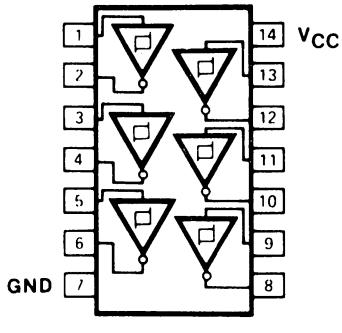
TRUTH TABLE

INPUT	OUTPUT
A	Y
H L	H L

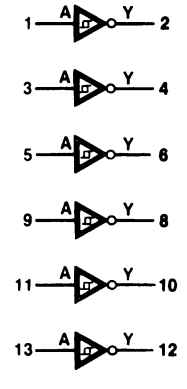
H = HIGH voltage level
L = LOW voltage level

7414 • 74LS14 • 74F14
HEX INVERTER SCHMITT TRIGGER

PIN ASSIGNMENT



LOGIC DIAGRAM



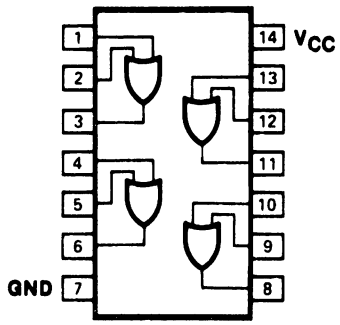
TRUTH TABLE

INPUT	OUTPUT
A	Y
0 1	1 0

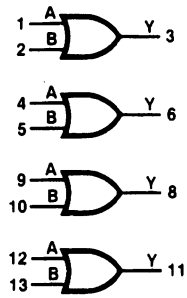
H = HIGH voltage level
L = LOW voltage level

7432 • 74S32 • 74LS32 • 74F32
QUAD 2-INPUT OR GATE

PIN ASSIGNMENT



LOGIC DIAGRAM



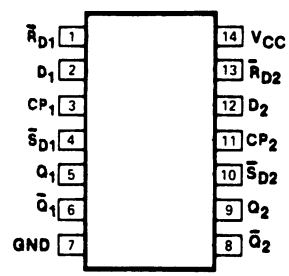
TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

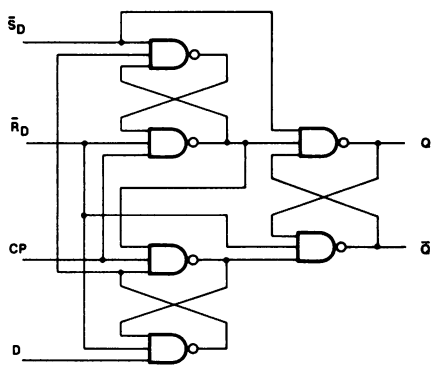
H = HIGH voltage level
L = LOW voltage level

7474 • 74S74 • 74LS74 • 74F74
DUAL D-TYPE FLIP FLOP (POSITIVE EDGE TRIGGERED)

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

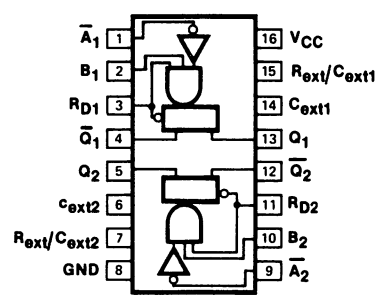
OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined[a]	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

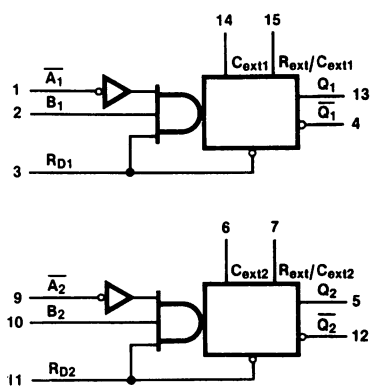
NOTE
(a) Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

74123 • 74LS123
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

PIN ASSIGNMENT



LOGIC DIAGRAM



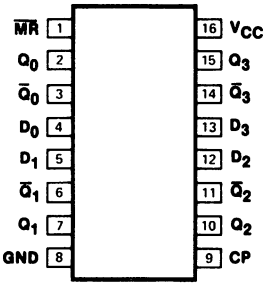
TRUTH TABLE

INPUTS			OUTPUTS	
R_D	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

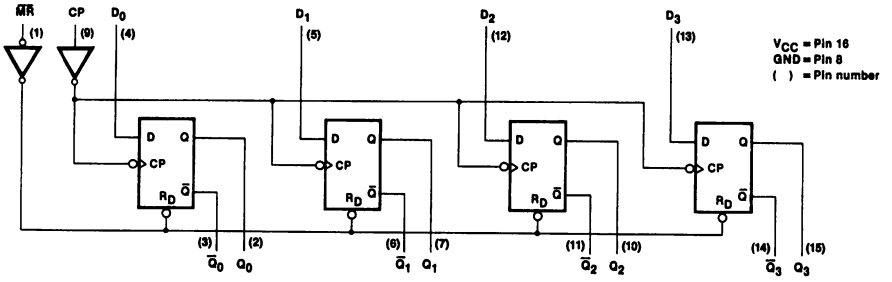
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = One HIGH-level pulse
⎍ = One LOW-level pulse

74175 • 74LS175 • 74F175
QUAD D-TYPE FLIP FLOP

PIN ASSIGNMENT



LOGIC DIAGRAM



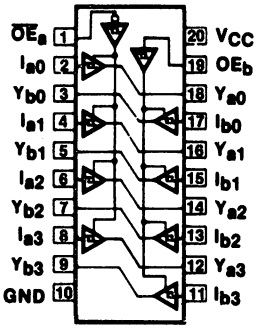
TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

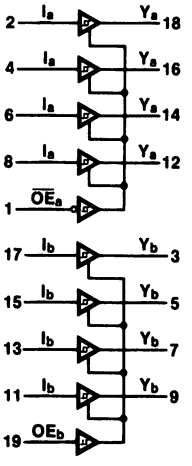
H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

74LS241 • 74F241
OCTAL BUFFER, TRI-STATE

PIN ASSIGNMENT



LOGIC DIAGRAM



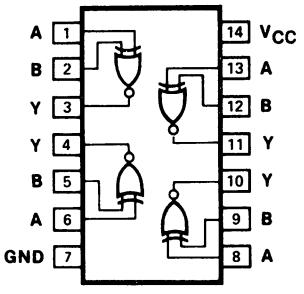
TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

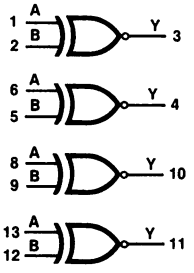
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

74LS266
QUAD 2-INPUT EXCLUSIVE NOR GATE (OPEN COLLECTOR)

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

PARTS LIST
PCB ASSEMBLY #310420

Commodore part numbers are provided for reference only and do not indicate the availability of parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Approved cross-references for TTL chips, Transistors, etc. are available in manual form through the Service Department, order part #314000-01. Unique or non-standard parts will be stocked by Commodore and are indicated on the parts list by a "C". Vendor Name and part number have been provided for your convenience in ordering custom or unique parts.

INTEGRATED CIRCUITS

U1	6502 CPU	C 901435-01
U2	23256 ROM	C 310654-03
U3	2016 RAM 200 NS	
U4	65SC22A VIA 2MHZ CMOS	C 310653-01
U5	Gate Array 20 Pin	C 251829-01
U6	Gate Array 40 Pin	C 251828-01
U7	R/W Hybrid	C 251853-01
U8	7406	
U9	65SC22A VIA 2MHZ	C 310653-01
U10	74LS74	
U11	WD 1770-00 Disk Control	C 310651-01 sub:
	WD 1772 Disk Control	C 310651-02
U12	74F32	
U13	74LS266	
U14	7407	
U15	74LS14	
U16	7406	
U17	74LS14	
U18	74LS175	
U19	74LS241	
U20	6526A CIA 2MHZ	C 906108-02 sub:
	8520 CIA 2MHZ	C 318029-02
U21	PST 520C/D Volt Detector	C 252034-02
U22	74LS123	

TRANSISTORS

Q1	MPSU51 PNP
Q2,3	2SC1815 NPN
Q4	2SA673 PNP
Q5	2SC945 NPN sub:
	2SC1685 R,S
Q7	2SC1815 NPN

DIODES

CR3-8	Signal 1N914
CR10	Signal 1N4002
CR11	Zener 3.3V

RESISTORS — All are carbon 1/4 watt, 5% unless noted

R1-3	47
R4	4.7K
R5	390 1/2W +/-5%
R6	1.2K
R7, 8	1K
R9-11	47K
R12	150
R13	390
R14, 15	2.7K
R16, 17	4.7K

RESISTORS (Continued)

R18, 19	47
R20	20K
R21	4.7K
R22	1K
R23	390
R24	47
R25-28	2K
R29	4.7K
R30	15K
R31	2K
R32	4.7K
R33-35	2.7K
R36-38	1K
R39	43K
R40	4.7K

CAPACITORS

C1-20	Ceramic	.1μF	16V
C21	Electrolytic	10μF	25V
C22, 23	Ceramic	.1μF	16V
C24	NPO	100pF	50V +/−5%
C27	Ceramic	.1μF	16V
C28	Elect	47μF	10V +50%, −10%
C29	Electrolytic	10μF	25V
C31	Electrolytic	1μF	16V
C32	Ceramic	.01μF	50V
C33	Tantalium	1μF	35V +/−10%

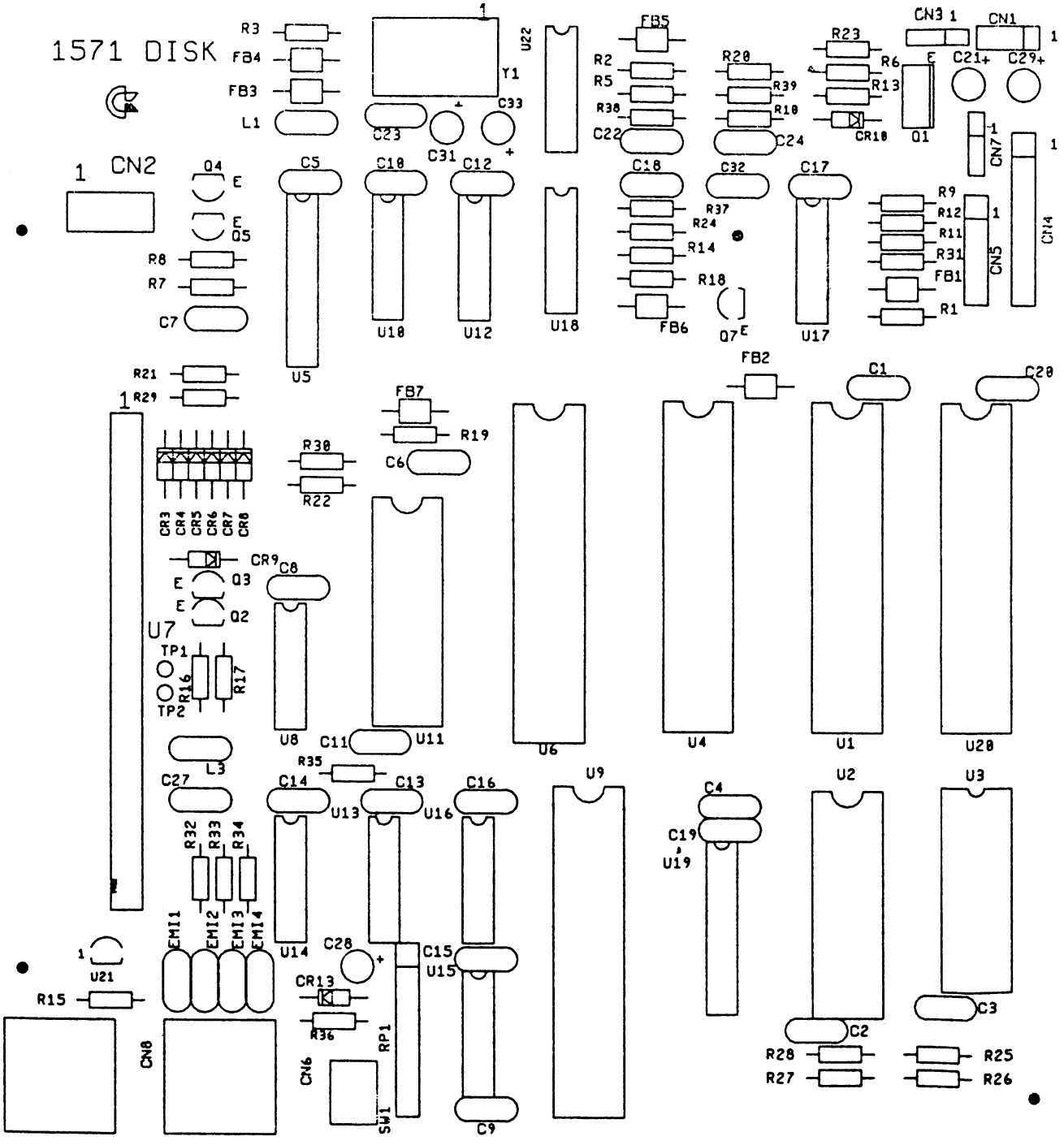
MISCELLANEOUS

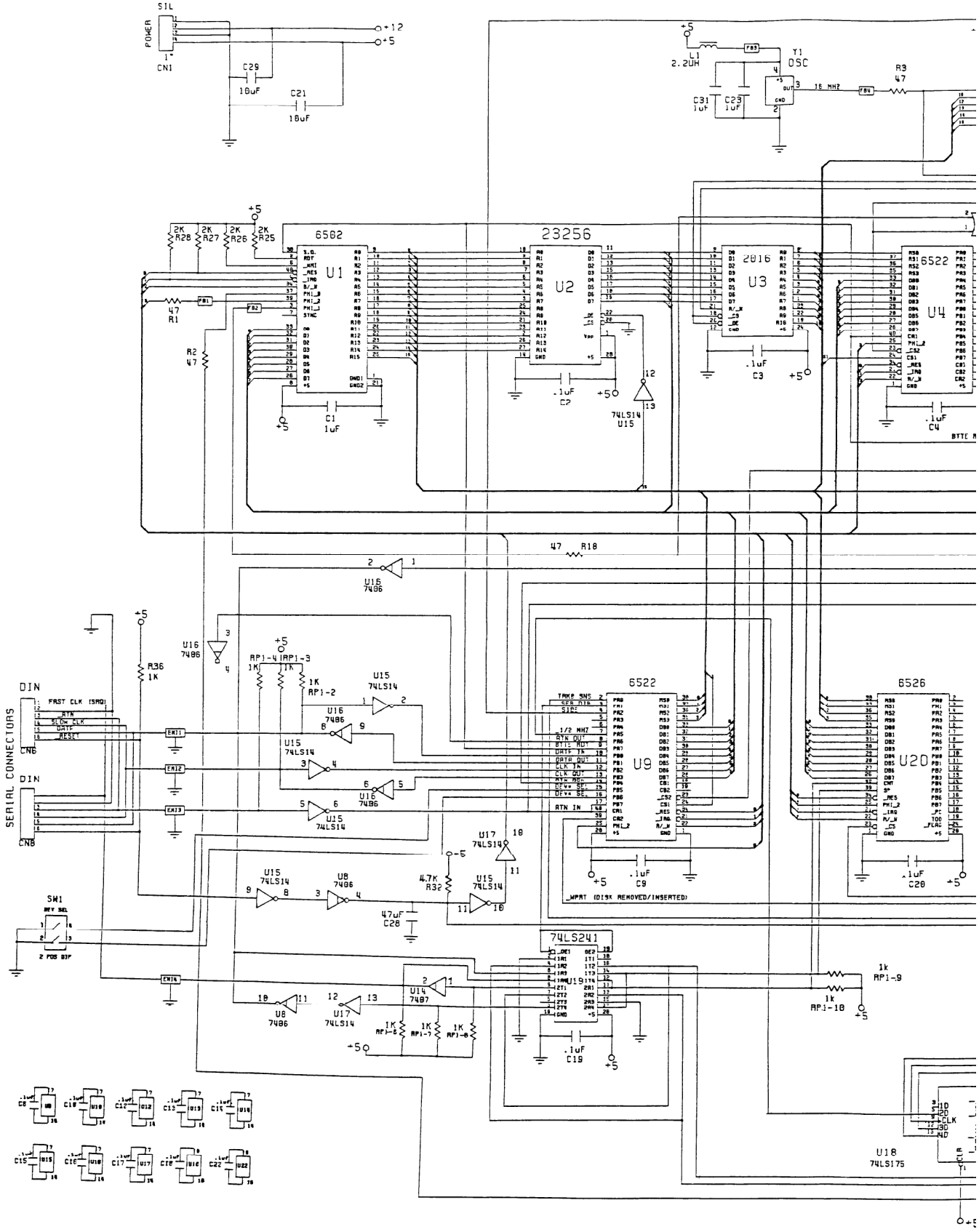
EMI 1-4	Ferrite Bead	
FB1-7	Ferrite Bead	
L1	Coil Inductor 2.2μH	
L3	Coil Inductor 100μH	
RP1	Resistor Pack 1K, 10Pin	
SW1	4 Pos Dip Switch	C 252144-02
Y1	Crystal Module 16MHZ	C 325566-01

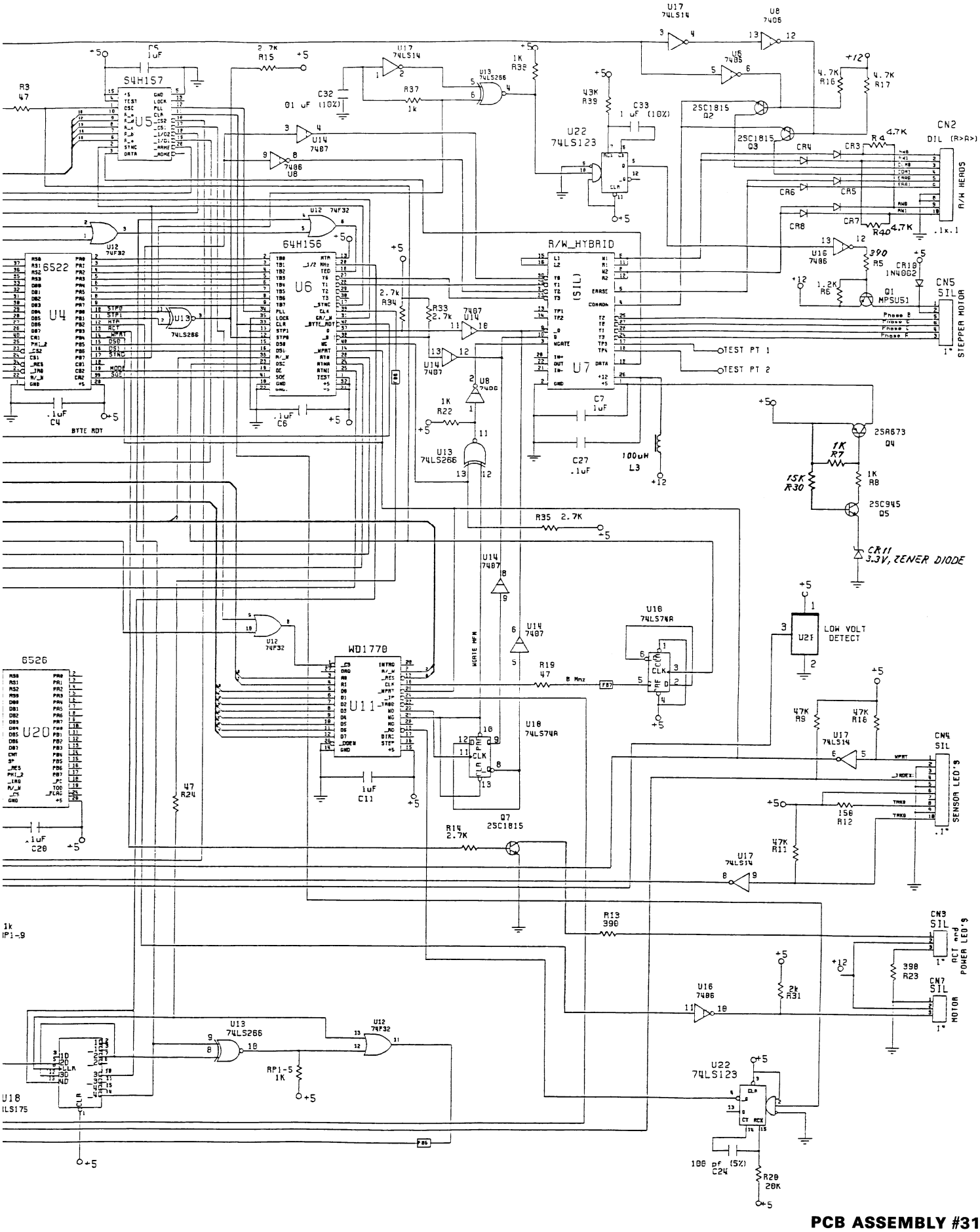
CONNECTORS

CN1	Header Assy, 4Pin (Molex 3022-04A, AMP 640098-4)
CN2	Header Assy, Dual RT Angle 10Pin
CN3	Header Assy, 3Pin (Molex 3022-03A, AMP 640098-3)
CN4	Header Assy, 10Pin (Molex 3022-10A, AMP 1-640098-0)
CN5	Header Assy, 6Pin (Molex 3022-06A, AMP 640098-6)
CN6, 8	Connector, 6Pin Din, Shielded C252166-01
CN7	Header Assy, 3Pin (Molex 3022-03A, AMP 640098-3)

PCB ASSEMBLY #310420
BOARD LAYOUT




POWER
CN1
C29
10uF
C21
10uF
+12
+5
L1
2.2UH
Y1
OSC
16 MHZ
R3
47
C31
1uF
C23
1uF
6502
U1
23256
U2
2016
U3
6522
U4
R28
R27
R26
R25
2K
R1
R2
47
C1
1uF
.1uF
C2
C3
C4
74LS14
U15
U16
7486
R18
R36
1K
RP1-4
RP1-3
RP1-2
DIN
FAST CLK (SMD)
ATN
SLOW CLK
DATA
RESET
CN6
CN8
SERIAL CONNECTORS
EXT1
EXT2
EXT3
EXT4
U9
U20
6526
RTN IN
_WPRT (DISK REMOVED/INSERTED)
C9
C20
U17
74LS14
U8
7486
4.7K
R32
47uF
C28
SW1
KEY SEL
2 POS DIP
74LS241
U19
U14
7407
1K
RP1-9
RP1-10
RP1-8
RP1-7
RP1-6
C19
U18
74LS175
C5
C11
C12
C13
C14
C15
C16
C17
C18
C22



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